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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. 13270US01)

IN THE APPLICATION OF:

D. Hylands et al.

SERIAL NO.: 10/032,667

FILED: October 24, 2001

FOR: TRANSFERRING DATA ALONG WITH CODE FOR PROGRAM OVERLAYS

ART UNIT: 2126

EXAMINER: T.T. Ho

Conf. No.: 7248

CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being sent via facsimile to the United States Patent and Trademark Office on May 8, 2006.

By: John A. Wiberg
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Applicant requests review of the final rejection in the above-identified application, stated in the final Office Action mailed on March 7, 2006 (hereinafter, the Final Office Action). No amendments are being filed with this request.

This request is being filed with a Notice of Appeal. The review is being requested for the reasons stated on the attached sheets.

REMARKS

The present application includes pending claims 1-28, all of which have been rejected. In Item 3 of the Final Office Action, mailed on March 7, 2006, claims 1-28 were rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Nelson U.S. Patent 6,209,061.

Claim 1 is directed to "a method for generating program overlays from a sequence of program code" and includes the following steps:

> (a) breaking the sequence of program code into a set of segments, wherein each segment contains a certain amount of related code for processing;
> (b) running a code segment in the set through a linker device;
> (c) extracting the code segment and related data segment produced by the linker device, with each associated pair of code and data segments representing an overlay;
> (d) checking if more segments exist in the set, if yes, then return to step (b), else proceed to step (e); and
> (e) concatenating the associated code and data segments into paired sets which can be referenced by the overlay manager.

Thus, steps (b) through (d) allow for the creation of multiple overlays, each comprising code and the data associated with that code, by utilizing multiple passes of the linker on multiple segments of code. The Examiner acknowledges that the Admitted Prior Art (APA) does not teach the use of multiple passes of a linker on the segments of code. The Examiner asserts that this aspect of the present invention is taught by Nelson. Applicant respectfully submits that Nelson says nothing about the process of generating overlays. Rather, Nelson merely talks about a method of using overlays. Therefore, Applicant submits that Nelson does not teach any of the steps of claim 1. In particular, Nelson does not teach utilizing multiple passes of a linker on multiple segments of code. The Examiner apparently asserts that this aspect of the present invention is disclosed by Nelson at col. 3, lines 9-19. Again, Applicant submits that this excerpt (nor any other excerpt) of Nelson does not even address a method of generating overlays. In particular, this excerpt (nor any other excerpt) does not say anything about using a linker, let alone anything about using multiple passes of a linker to generate overlays. Furthermore the

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overlays used in Nelson contain only data and parameters. See col. 3, lines 6-9. This is in contrast to the overlays generated by the method of claim 1, wherein the overlays comprise both code and data.

The Examiner also acknowledges that the Admitted Prior Art (APA) does not teach concatenating step (e). The Examiner asserts that this aspect of the present invention is taught by Nelson at col. 3, lines 10-19. The Examiner asserts that the fact that "the overlay memory 23 can be segmented into a number of memory regions, with each region defined by a base pointer value" somehow teaches concatenating together associated code and data segments into paired sets. Applicant submits again that the overlays of Nelson consist only of data and parameters, rather than code and data (col. 3, lines 6-9). Therefore, Nelson cannot teach concatenating step (d). Furthermore, Nelson only talks about using overlays, and does not describe a method of generating said overlays.

For at least the reasons outlined above, Applicant submits that claim 1, and claims 2-11 depending therefrom, are not taught by the combination of the admitted prior art and Nelson.

Claim 12 contains some limitations that are similar to claim 1. For example, steps (e) through (g) allow for the creation of multiple overlays, each comprising code and the data associated with that code, by utilizing multiple passes of the linker on multiple segments of code. The Examiner acknowledges that the Admitted Prior Art (APA) does not teach the use of multiple passes of a linker on the segments of code, nor concatenating step (h). The Examiner asserts that these aspects of the present invention are taught by Nelson. Applicant respectfully disagrees and submits that claim 12 is allowable for at least the reasons set out above with respect to claim 1. Thus, Applicant submits that claim 12, and claims 13-18 depending therefrom, are not taught by the combination of the admitted prior art and Nelson.

Claim 19 was also rejected over the combination of the APA and Nelson. The Examiner acknowledges on page 8 of the Final Office Action that the APA does not teach step (b): "creating an overlay control file for each overlay, whereby the overlay control file describes each pair of code and data associated with each overlay." The

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Examiner asserts on page 9 of the Office Action that step (b) is taught by Nelson at column 4, lines 5-10. Column 4, lines 5-10, of Nelson refer to an overlay memory controller 24, which holds the respective base pointers of the subregions of the overlay memory 23. Applicant submits that this overlay memory controller 24 does not constitute an overlay control file for each overlay, and in particular, an overlay control file that describes each pair of code and data associated with each overlay, as called for in claim 19. Applicant further points out that the overlays of Nelson consist of data only. See column 3, lines 6-9, which say, "Overlay memory 23 is a relatively small, high-speed memory which provides storage for data and parameters that are temporarily required for a program 26 that is currently running on CPU 12." In contrast, the overlays of the present invention comprise both code and data. On page 11 of the Office Action, in the "Response to Arguments" section, the Examiner asserts that APA was used to teach this limitation. However, step (b) claims "creating an overlay control file" that "describes each pair of code and data associated with each overlay." The Examiner explicitly acknowledges that this step is not taught by the APA. Therefore, Applicant submits that step (b) is not taught by the APA nor by Nelson.

Further regarding claim 19, the Examiner asserts that step (c), "generating a wrapper file from the overlay control file," is taught by the APA at paragraphs 13 and 15. Applicant submits that while these paragraphs refer generically to a wrapper, they do not describe generating a wrapper file from an overlay control file.

The Examiner further asserts regarding claim 19 that step (d), "creating a linker command file for the common area," is taught by the APA at paragraph 13. Applicant submits that paragraph 13 of the present application says nothing about a linker command file and, more particularly, says nothing about a linker command file for the common area.

The Examiner further asserts regarding claim 19 that step (e), "creating a linker command file for the overlay area," is taught by the APA at paragraph 13. Applicant submits that paragraph 13 of the present application says nothing about a linker command file and, more particularly, says nothing about a linker command file for the overlay area.

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Further regarding claim 19, the Examiner asserts that step (f), "performing an initialization for the overlay," is taught by the APA at paragraph 15. Applicant submits that paragraph 15 says nothing about performing an initialization for an overlay. Applicant further submits that performing step (f) is performed in the generating of the overlays, as indicated in the preamble of claim 19. Paragraph 15 talks about using overlays, but does not say anything about the process of generating said overlays.

The Examiner further asserts regarding claim 19 that step (j), "producing a load command file, whereby the command file will load the overlay sections file into the appropriate receiving area," is taught by the APA at paragraph 16. Applicant submits that paragraph 16 of the present application says nothing about a load command file.

For at least the reasons outlined above, Applicant submits that claim 19, and claims 20-28 depending therefrom, are not taught by the combination of the admitted prior art and Nelson.

In view of the foregoing, Applicant respectfully submits that claims 1-28 of the present application should be in condition for allowance at least for the reasons discussed above and request that the outstanding rejections be reconsidered and withdrawn. The Commissioner is authorized to charge any necessary fees or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

Date: 5/8/06

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